

DC-DC converter

The invention relates to a DC-DC converter, a controller for use in the DC-DC converter, an apparatus comprising the DC-DC converter, and a method of controlling the DC-DC converter.

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US 6,366,070 discloses a switching voltage regulator which employs a dual modulation scheme to control the regulator's switching components. A control circuit indirectly monitors the load current. When the load decreases, the control circuit reduces both the duty ratio and the frequency of the control signals which operate the switching transistors, thereby maintaining a high efficiency level over a wider output current range than can be achieved with fixed-frequency control signals. This control can be applied to switching regulators using peak current mode, average current mode, or voltage mode control, as well as buck, buck-boost, and boost power stages.

The prior art DC-DC converter has a limited control range when the duty ratio is small.

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It is an object of the invention to provide a DC-DC converter which is able to cope with larger dynamic load variations. The invention is defined by the independent claims. Advantageous embodiments are defined in the dependent claims.

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The DC-DC converter in accordance with the invention comprises a switch for periodically connecting an inductor to a DC-input voltage during an on-period of a period time. The operating frequency of the DC-DC converter is the inverse of the period time. The DC-DC converter further has an output which is coupled to the inductor and at which the output voltage is present. The current through the inductor increases during the on-period to store energy in the inductor. During the off-period, energy is supplied by the inductor to the load and the current in the inductor decreases.

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A controller controls the operating frequency to be substantially proportional to the output voltage to obtain a substantially constant average duration of the on-period as

function of the output voltage. The average duration of the on-period will be selected to be large enough to allow the on-time to become smaller during a short period in time when the load requires less current and the frequency of the converter is not instantly controlled to cope with the lower current. If in the prior art the duty cycle (and thus the on-time) is controlled to become smaller (it is disclosed that the duty cycle may become zero) the duty becomes too small to cope with dynamic load variations.

The operating frequency need not be exactly proportional to the output voltage as it is not required that the average value of the on-period has exactly a predetermined duration. It suffices that the output voltage is substantially proportional such that the average value of the on-period is substantially constant.

In the DC-DC converter in accordance with the invention, the duration of the on-period is substantially independent on the output voltage and thus can be selected large enough to cope with dynamic load variations at the output.

Further, in the prior art mentioned, it is not the output voltage which is directly controlling the operating frequency of the DC-DC converter, but the difference of the output voltage and a reference voltage.

In an embodiment as defined in claim 2, the DC-DC converter comprises a controllable oscillator which supplies a control signal to a drive circuit. The drive circuit supplies a drive signal to the switch to control on- and off-states of the switch.

An output voltage measurement circuit supplies an oscillator control signal to the controllable oscillator to adapt its operating frequency to be substantially proportional to the output voltage while keeping the on-period of the switch substantially constant. Such a drive circuit, controllable oscillator, and output voltage measurement are generally known. Their implementation is not relevant to the invention. But, the transfer characteristic should be selected such that the operating frequency depends in the desired manner from the output voltage. The output measurement circuit may supply the output voltage as the oscillator control signal.

In an embodiment as defined in claim 3, the operating frequency is substantially directly proportional to the output voltage. This is a simple approach, the operating frequency changes substantially linear with the output voltage:  $f_o = k_1 \times V_o$ , wherein  $f_o$  is the operating frequency,  $k_1$  is a constant, and  $V_o$  is the output voltage.

In an embodiment as defined in claim 4, the operating frequency is further dependent on the DC-input voltage to keep the duration of the on-period substantially constant at a varying input voltage.

In an embodiment as defined in claim 5, the operating frequency is substantially directly proportional to the inverse of the DC-input voltage.

In an embodiment as defined in claim 6, the dependency of the operating frequency on the output voltage and the DC-input voltage is according the following equation

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$$f_o = (N \times V_o) / (T_{on} \times V_i)$$

wherein N is a constant,  $V_o$  is the output voltage,  $T_{on}$  is the substantially constant on-period, and  $V_i$  is the DC-input voltage. This dependency is especially relevant in a buck converter wherein the duty cycle in the steady state is determined by the following equation

$$d = T_{on} / T_p = V_o / V_i$$

10 wherein  $T_p$  is the duration of one period containing one on-period  $T_{on}$  and one off-period  $T_{off}$ , and thus is the inverse of the operating frequency  $f_o$ .

In an embodiment as defined in claim 8, the controller comprises a comparator which compares an actual duration of the on-period of the switch with a desired duration of the on-period to control the operating frequency to obtain a substantially constant average  
15 duration of the on-period. Only the desired average on-time needs to be set, it is not required to measure the value of the DC-input voltage and the value of the output voltage. It is further an advantage that tolerances in the controller will be negotiated by the closed loop.

Preferably, the controller further comprises a loop filter which low pass filters the difference between the actual duration of the on-period and the desired duration of the on-period and  
20 which supplies the filtered difference to the controllable oscillator. Preferably, an integration time of the filter is substantially longer than the duration of one period to obtain a slow loop to prevent instabilities. The loop need not be very fast because it only has to control the operating frequency such that the duration of the on-period is in average constant. Dynamic variation of the duration of the on-time with dynamic load steps is allowable.

25 In an embodiment as defined in claim 9, on top of the presence of the loop, also the value of the DC-input voltage and the value of the output voltage is measured to obtain a fast reaction on variations on these voltages.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

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In the drawings:

Fig. 1 shows a block diagram of an embodiment of a DC-DC converter in accordance with the invention,

Fig. 2 shows a block diagram of a buck converter in accordance with the invention,

Figs. 3 show signals for elucidating the operation of the buck converter of Fig. 2,

Fig. 4 shows the operating frequency as a function of the output voltage,

Fig. 5 shows an embodiment of a control circuit for controlling the buck converter of Fig. 2, and

Fig. 6 shows another embodiment of a control circuit for controlling the buck converter of Fig. 2.

The same references in different Figs. refer to the same signals or to the same elements performing the same function.

Fig. 1 shows a block diagram of an embodiment of a DC-DC converter in accordance with the invention. The DC-DC converter comprises a series arrangement of an inductor L and a controllable switch S1. The series arrangement receives a DC-input voltage  $V_i$ . The negative pole of the DC-input voltage  $V_i$  is connected to ground. A diode D is arranged between an output O1 and the junction of the inductor L and the switch S1. Both a smoothing capacitor C and a load Z are arranged between the output O1 and ground. The output voltage  $V_o$  of the DC-DC converter is present across the load Z. A control circuit CO receives the output voltage  $V_o$  and supplies a control signal CS to the switch S1 to control the on- and off-periods  $T_{on}$ ,  $T_{off}$  of the switch S1.

The controller CO controls the operating frequency of the DC-DC converter as a function of the output voltage  $V_o$  such that the on-period  $T_{on}$  is kept substantially constant. Embodiments of the controller CO are elucidated with respect to Figs. 5 and 6.

The DC-DC converter shown may be build in an electronic apparatus such as for example, a television receiver, a computer monitor, a video cassette recorder, a printer, or a computer. The load Z is a circuit of this electronic apparatus.

In an embodiment in accordance with the invention, the controller CO receives the input voltage  $V_i$  to further control the operating frequency  $f_o$  as a function of the input voltage  $V_i$  such that the on-period  $T_{on}$  is kept substantially constant.

Fig. 2 shows a block diagram of a buck converter in accordance with the invention. The buck converter comprises a series arrangement of main current paths of a switch S1 and a switch S2 arranged to receive the DC-input voltage  $V_i$ . An inductor L1 is

arranged between the output O1 of the DC-DC converter and the junction of the main current paths of the switches S1 and S2. The negative pole of the DC-input voltage and the terminal of the switch S2 not connected to the switch S1 are grounded. A parallel arrangement of a smoothing capacitor C and a load Z is arranged between the output O1 and the ground.

5 The control circuit CO receives the output voltage  $V_o$ , and optionally the input voltage  $V_i$  to supply the control signals CS1 and CS2 which control the on- and off-periods of the switches S1 and S2, respectively. The switches S1 and S2 are controlled to have substantially opposite phases: when the switch S1 is conductive (closed) the switch S2 is non-conductive (open), and the other way around.

10 Again, the controller CO controls the operating frequency  $f_o$  of the DC-DC converter as a function of the output voltage  $V_o$  such that the on-period  $T_{on}$  of the switch S1 is kept substantially constant. Embodiments of the controller CO are elucidated with respect to Figs. 5 and 6. In an embodiment in accordance with the invention, the controller CO receives the input voltage  $V_i$  to further control the operating frequency  $f_o$  as a function of the  
15 input voltage  $V_i$  such that the on-period  $T_{on}$  is kept substantially constant as a function of the input voltage  $V_i$  also. The output current  $I_O$  is the current required by the load Z.

Again, the buck converter may be build in an electronic apparatus such as for example, a television receiver, a computer monitor, a video cassette recorder, a printer, or a computer. The load Z is a circuit of this electronic apparatus. The buck converter may be  
20 particularly advantageously used to regulate the supply voltage of a microprocessor. In today's computers, the microprocessor requires very high currents at a power supply voltage of approximately 1.5 Volts. Usually, the converter has a DC-input voltage of about 12 Volts. The current demanded by the microprocessor varies to a very large amount while the power supply voltage should be well defined.

25 Figs. 3 show signals for elucidating the operation of the buck converter of Fig. 2. Fig. 3A shows the control signal CS1, Fig. 3B shows the control signal CS2, and Fig. 3C shows the current  $I_L$  through the inductor L.

30 At instant  $t_1$ , which is the start of the on-period  $T_{on}$  of the switch S1, the switch S2 is opened and the switch S1 is closed, the inductor L is connected to the positive pole of the DC-input voltage  $V_i$  which has higher value than the output voltage  $V_o$ , and thus the current  $I_L$  will start to increase. If both the DC-input voltage  $V_i$  and the output voltage  $V_o$  are substantially constant, the current  $I_L$  will increase substantially linearly.

At instant  $t_2$ , which is the end of the on-period  $T_{on}$  of the switch  $S_1$ , the switch  $S_1$  is opened and the switch  $S_2$  is closed. Now, the voltage over the inductor  $L$  changes polarity and the current  $I_L$  starts to decrease. If the output voltage  $V_o$  is considered to be substantially constant, the current  $I_L$  through the inductor  $L$  will decrease substantially linearly. At instant  $t_3$  a next on-period  $T_{on}$  of the switch  $S_1$  starts. The off-period of the switch  $S_1$  lasts from instant  $t_2$  to instant  $t_3$ . The duration of one period  $T_p$  of a switching cycle is referred to as the period duration  $T_p$ . The operating frequency  $f_o$  of the buck converter is the inverse of the period duration  $T_p$ .

If the amount of energy required by the load  $Z$  decreases, the output voltage  $V_o$  starts rising because energy will be stored in the smoothing capacitor  $C$ . The controller  $CO$  controls the average operating frequency  $f_o$  of the buck converter such that the average on-time  $T_{on}$  of the switch  $S_1$  is kept constant.

In a buck converter, the operating frequency  $f_o$  depends on the value of the DC-input voltage  $V_i$  and the output voltage  $V_o$  in accordance with the following equation

$$f_o = (N \times V_o) / (T_{on} \times V_i)$$

wherein  $T_{on}$  is the substantially constant on-time, and  $N$  is the number of buck converters if multiple buck converters are arranged in parallel to minimize the ripple on the output voltage  $V_o$ .

Thus, based on this equation, the controller  $CO$  adapts the operating frequency  $f_o$  with the value of the output voltage  $V_o$  and the value of the DC-input voltage  $V_i$  while the value of the on-period  $T_{on}$  is kept fixed.

Fig. 4 shows the operating frequency as a function of the output voltage.

The operating frequency  $f_o$  of the buck converter is depicted along the vertical axis and the output voltage  $V_o$  is depicted along the horizontal axis.

In Fig. 4, by way of example, two graphs  $f_{l1}$  and  $f_{l2}$  are shown of the operating frequency  $f_o$  as function of the output voltage  $V_o$ . For the ease of explanation, it is assumed that the DC-input voltage  $V_i$  does not vary.

In practical applications, often the DC-input voltage  $V_i$  is fixed but may have different discrete values of, for example, 12 Volts or 5 Volts. In this case it is not necessary to measure the value of the DC-input voltage  $V_i$  accurately, and it can be treated as a constant for which different values can be selected according to the actual value of the DC-input voltage  $V_i$ .

The graph fl1 shows that the operating frequency  $f_o$  decreases linearly with decreasing output voltage  $V_o$ . Below a particular value  $V_{o2}$  of the output voltage  $V_o$ , the operating frequency should be limited to a particular minimum value  $f_{min}$  to guarantee start-up of the converter. It is also possible to select a frequency offset  $FO$  on the operating frequency  $f_o$  such that  $f_{min}$  is reached at the minimum value  $V_{o1}$  of the output voltage  $V_o$ , as is indicated by the line fl2. The minimum frequency  $f_{min}$  or the offset  $FO$  is selected according to the desired minimum duration of the on-time  $T_{on}$  (the maximum value of this minimum frequency  $f_{min}$ ) and an acceptable maximum peak current (the minimum value of this minimum frequency) leading to a maximum on-time  $T_{on}$ .

Fig. 2 shows the principal diagram of buck converter wherein the switch  $S_1$  is usually a FET called control-FET or control switch and the synchronous switch  $S_2$  is usually a FET called sync-FET or sync switch. Usually, the current through the switch  $S_1$  is sensed with a sense-resistor (not shown) which usually is arranged between the positive pole of the DC-input voltage  $V_i$  and the switch  $S_1$ . With the buck converter operating with (direct) current mode control, a minimum on-time  $T_{on}$  is necessary to be able to measure the current in the inductor  $L$  during the on-time  $T_{on}$  of the switch  $S_1$ . Parasitic capacitances or delays will disturb the sense signal considerably if the on-time  $T_{on}$  of the switch  $S_1$  becomes very short.

A buck converter as such is disclosed in US-A-4,524,412. In a buck converter the duty cycle of the switching node is a function of output voltage  $V_o$  and input voltage  $V_i$ . When a large ratio between the supply voltage  $V_i$  and the output voltage  $V_o$  is applied in a buck converter very small on-times  $T_{on}$  of the control switch  $S_1$  can occur. If current mode control is applied the measured inductor current  $I_L$  at the end of the control switch  $S_1$  on-time  $T_{on}$  can therefore be disturbed by parasitic components or not settled in time.

According to the basic equation of a buck converter, the duty cycle  $d$  in the steady state is a function of the DC-input voltage  $V_i$  and the output voltage  $V_o$ :

$$d = T_{on} / T_p = V_o / V_i$$

wherein  $T_p$  is the period duration and  $1 / T_p$  is the operating frequency  $f_o$ .

If a multitude of buck converters is arranged in parallel to minimize the ripple on the output voltage  $V_o$ , the buck converters are controlled to be active sequentially each one during its own phase. For example, with respect to Fig. 3, if two buck converters are used in parallel, in one period  $T_p$ , the first buck converter starts an on-phase at the instant  $t_1$  as shown, another one of the buck converters starts an on-phase at instant  $t_5$ . This dual buck converter system has two phases, one for each buck converter. In such a system of a

multitude of buck converters,  $d$  is the duty cycle at the switching node of a phase (one of the buck converters), and  $T_p$  is the period time of the signal at the switching node of each phase.

In case of a low output voltage  $V_o$ , for example during start-up of the converter, or over-current protection, problems can occur if the on-time  $T_{on}$  cannot be

5 lowered: the converter will not be regulated anymore.

If  $T_{on}$  cannot become lower than a minimum on-time  $T_{min}$ , at a particular output voltage  $V_o$  and input voltage  $V_i$ , in a buck converter, the operating frequency  $f_o$  has to be lowered to keep the buck converter regulated.

As the current ripple  $I_r$  in the steady state is equal to the delta of the current  $I_L$  through the inductor  $L$  during the on-period of the switch  $S_1$ , this ripple can be calculated as:

$$I_r = (V_i - V_o) \times (T_{on} / L).$$

Thus, at a longer period time  $T_p$  than necessary, the system operates with a longer on-time  $T_{on}$  of the switch  $S_1$  than necessary and thus the current ripple  $I_r$  will be larger than necessary. Therefore, an optimum choice for the current ripple  $I_r$ , is to select the on-time  $T_{on}$  as short as possible. The minimum period time  $T_p$  then must be:

$$T_p = T_{on} \times (V_i / V_o)$$

An existing method of adapting the period time  $T_p$ , as disclosed in US 4,524,412, is to measure the current during the on-time of the switch  $S_2$  and to prevent the switch  $S_1$  to switch on until the current in the switch  $S_2$  has decreased below a particular maximum value. This prior art has the drawback that it is necessary to measure the current during the on-time of the switch  $S_2$ .

In the present application, a method is described to keep the on-time  $T_{on}$  of the control switch  $S_1$  rather constant over the whole output voltage- and input voltage range. With the proposed solution, the output voltage range can be made larger, and smaller inductors  $L$  and output capacitors  $C$  can be chosen, without the need of current sensing during the sync switch  $S_2$  stroke. The output capacitors  $C$  can be selected as small as possible because the ripple current  $I_r$  in the inductor  $L$  is minimized. Advantageously, frequency adaptation is a function of the input voltage  $V_i$  and output voltage  $V_o$ . The output voltage  $V_o$  of the buck converter can be adapted over a very wide range without significant change in the ripple current  $I_r$  and with almost constant on-time  $T_{on}$  of the control FET  $S_1$ . Constant on-time of the control FET  $S_1$  is an advantage because larger on-time variations caused by dynamic load variations are possible.

In a practical buck converter, a fixed frequency is used for normal operation from no load to a particular value of the output current  $I_o$  supplied to the load  $Z$ . The period



time  $T_p$  is selected such that the on-time  $T_{on}$  is larger than  $T_{min}$  so that during load-steps the on-time  $T_{on}$  can still be lowered to keep the converter regulated. Below a predetermined value of the output voltage  $V_o$ , the operating frequency  $f_o$  will be lowered according to the equation valid for the buck converter. This means that the operating frequency  $f_o$  will be proportional to the output voltage  $V_o$  and the conversion factor can be defined or kept fixed with the combination of the number of phases  $N$  and the DC-input voltage  $V_i$ . The current mode loop operates as usual and will keep the on-time  $T_{on}$  almost constant as it tries to keep the peak-current  $I_r$  constant.

It is also possible to adapt the frequency  $f_o$  over the whole range of the output voltage  $V_o$ . This is even simpler because it is not required to detect whether the output voltage  $V_o$  drops below the predetermined value.

It is also possible to define a desired on-time  $T_{od}$  that is a factor times the minimum on-time  $T_{min}$ . This factor can be fixed or externally tuned. During operation, the desired on-time  $T_{od}$  (see Fig. 6) is compared with the actual on-time  $T_{om}$  and with a slow loop the on-time is adapted to become equal to the desired on-time  $T_{od}$ . As a result, the operating frequency  $f_o$  is automatically adapted to the maximum value possible at the given desired on-time  $T_{od}$ . The advantage of this solution is that the operating frequency  $f_o$  will always be the maximum possible frequency under all circumstances, and that it is not necessary to measure the DC-input voltage  $V_{in}$  accurately. If 5 Volts or 12 Volts operation is desired, only two fixed values for the DC-input voltage  $V_{in}$  are sufficient because of the automatic adaptation. Also the number of phases  $N$  can be programmed in the conversion factor of the oscillator OSC.

Fig. 5 shows an embodiment of a control circuit for controlling the buck converter of Fig. 2. The control circuit CO comprises an output voltage measurement circuit OVM, a controllable oscillator COS, and a driver DR.

The output voltage measurement circuit OVM has an input to receive the output voltage  $V_o$ , an input to receive the predetermined value  $V_{o2}$  (see Fig. 4, the line fl1) of the output voltage  $V_o$  at which the control mode changes, and an output to supply the oscillator control signal OV. The output voltage measurement circuit OVM may comprise a comparing circuit (not shown) which compares the output voltage  $V_o$  with the predetermined value  $V_{o2}$  to supply the oscillator control signal OV which is the minimum of the output voltage  $V_o$  or the predetermined value  $V_{o2}$ . The output measurement circuit OVM may also directly supply the output voltage  $V_o$  as the oscillator control signal OV.

The controllable oscillator COS receives the oscillator control signal OV to supply the control signal OCS to the drive circuit DR. The controllable oscillator may be a known voltage to frequency converter. The control signal OCS will have a repetition frequency which is proportional to the level of the oscillator control signal OV:

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$$f_{osc} = a \times OV$$

wherein  $f_{osc}$  is the repetition frequency of the control signal OCS,  $a$  is a constant factor, and OV is the level of the oscillator control signal OV.

The driver DR receives the control signal OCS and supplies the drive signal CS1 to control the on- and off periods of the switch S1, and the drive signal CS2 to control the on- and off periods of the switch S2. The period time  $T_p$  which contains one on- and off period  $T_{on}$ ,  $T_{off}$  is the inverse of the repetition frequency  $f_{osc}$  of the control signal OCS. For example, in a practical implementation, the control signal OCS may be a pulse signal with a rising edge which indicates the start of the on-period  $T_{on}$  of the switch S1. The substantially fixed on-time  $T_{on}$  may already be provided in the control signal OCS, or may be counted in the driver DR. The on-time  $T_{on}$  of the switch S1 may be counted by a counter (not shown) which counts clock pulses of a clock generator in a known manner. The drive signal CS2 is in principle the inverse of the drive signal CS1. As known, care has to be taken that the switches S1 and S2 do not conduct at the same time.

Below the predetermined value  $V_{o2}$ , the buck converter operates at a fixed operating frequency  $f_{min}$  as the oscillator signal OV is the predetermined value  $V_{o2}$ , above the predetermined value  $V_{o2}$ , the converter operates in the constant on-time  $T_{on}$  mode wherein the operating frequency  $f_o$  is proportional to the value of the output voltage  $V_o$ .

Fig. 6 shows another embodiment of a control circuit for controlling the buck converter of Fig. 2. The controller CO comprises a comparator DCO, a loop filter INT, a controllable oscillator OSC, a drive circuit DR, an output voltage measurement circuit OVM, and an input voltage measurement circuit IVM. Usually, the loop filter INT is a low pass filter and comprises an integrator.

The comparator DCO compares the measured actual on-period  $T_{om}$  with a desired on-period  $T_{od}$  and supplies a difference signal DI.

The loop filter INT filters the difference signal DI to obtain the filtered difference signal IDI. Preferably, an integrating period of the filter INT is much longer than the period time  $T_p$ .

The output voltage measurement circuit OVM receives the output voltage  $V_o$  and measures the value  $V_{Vo}$  of the output voltage  $V_o$ . The output voltage measurement circuit OVM may transfer the output voltage  $V_o$  to its output such that the value  $V_{Vo}$  is the output voltage  $V_o$ . In the last case, the output voltage measurement circuit OVM is  
5 superfluous.

The input voltage measurement circuit IVM receives the input voltage  $V_i$  and measures the value  $V_{Vi}$  of the input voltage  $V_i$ . The input voltage measurement circuit IVM may transfer the input voltage  $V_i$  to its output such that the value  $V_{Vi}$  is the input voltage  $V_i$ . In the last case, the input voltage measurement circuit IVM is superfluous.

10 The measurement of the values  $V_{Vo}$  and  $V_{Vi}$  of the output voltage  $V_o$  and the input voltage  $V_i$ , respectively may be relevant if the oscillator OSC is controlled by a digital circuit which calculates the required operation frequency  $f_o$  from the digital values of the output voltage  $V_o$  and the input voltage  $V_i$ . The oscillator OSC may also be controlled by an analog circuit.

15 The oscillator OSC which receives the filtered difference signal IDI and the values  $V_{Vo}$  and  $V_{Vi}$  will supply an oscillator signal OS with a repetition frequency equal to the operation frequency  $f_o$  in accordance with the equation:

$$f_o = (k_c \times V_o) / (T_{od} \times V_i)$$

wherein the value of  $k_c$  depends on the filtered difference signal IDI.

20 Alternatively, only the desired on-time  $T_{od}$  needs to be set, it is not required to measure both the value of the DC-input voltage  $V_i$  and the value of the output voltage  $V_o$ . The closed loop obtained by the comparator DCO and the loop filter INT controls the operating frequency  $f_o$  to obtain a substantially constant average duration of the on-period  $T_{on}$  which is equal to the desired on-period  $T_{od}$ .

25 The closed loop has the advantage that tolerances in the controller CO will be negotiated by the closed loop.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative  
30 embodiments without departing from the scope of the appended claims.

For example, the inductor L which is shown to be a coil may be a transformer. A transformer is particular relevant if several different output voltage have to be generated, or when the primary side and the secondary side of the DC-DC converter must be galvanic separated.

The controlled switches are preferably semiconductor devices, such as MOSFETs or bipolar transistors.

This control in accordance with the invention can be applied to switching regulators using peak current mode, average current mode, or voltage mode control, as well  
5 as buck, buck-boost, and boost power stages.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of elements or steps other than those listed in a claim. The invention can be implemented by  
10 means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.